REMARKS

Applicants have amended their claims in order to further clarify the definition of various aspects of the present invention. Specifically, Applicants have amended the claims to consistently recite the first "insulation" film, and to consistently recite the "insulation" copper diffusion barrier film. In addition, Applicants have further amended claim 2 to recite that an "organic acid" cleaning treatment (e) is carried out to the upper surface of the first insulation film and an upper surface of the metal interconnect, after step (d) (the removing of the metal layer outside the interconnect groove); to recite that after step (e), a hydrogen anneal treatment (f) is carried out to the upper surface of the first insulation film and the upper surface of the metal interconnect; to recite that after step (f), a plasma treatment is carried out in a gas atmosphere including an ammonia gas, to the upper surface of the first insulation film and the upper surface of the metal interconnect; and to recite that an insulation copper diffusion barrier film is deposited by plasma chemical vapor deposition on the upper surface of the first insulation film and the upper surface of the metal interconnect film, treated by the organic acid cleaning treatment, the hydrogen anneal treatment and the plasma treatment. Note, for example, Embodiment 1 on pages 32-93 of Applicants' specification, together with Embodiment 6 on pages 109 and 110 thereof. Moreover, Applicants have cancelled claims 3-6 and 11-13 without prejudice or disclaimer; have amended claim 7 to be dependent on claim 2, and have further amended claim 7 to recite that the reducing process is carried out after step (d) and before step (e); and have further amended claim 16 to recite that the insulation copper diffusion barrier film is formed after step (g).

Furthermore, Applicants are adding new claims 18-20 to the application. Claims 18 and 19, each dependent on claim 2, respectively recites that citric acid is

applied during the organic acid cleaning treatment, and that a mixture of organic acid and hydrogen fluoride is applied during the organic acid cleaning treatment. Claim 20, also dependent on claim 2, recites that in this organic acid cleaning treatment any damaged layer in the upper surface is removed. Note, for example, page 110 of Applicants' specification.

Applicants respectfully submit that all of the claims presented for consideration by the Examiner patentably distinguish over the teachings of the references applied by the Examiner in rejecting claims in the Office Action mailed August 3, 2005, that is, the teachings of the U.S. patents to Mikagi, No. 6,274,923, to Ngo, et al., No. 6,303,505, and to Skee, et al., No. 5,989,353, under the provisions of 35 USC 103.

It is respectfully submitted that the references as applied by the Examiner would have neither taught nor would have suggested such a fabrication method as in the present claims, including, inter alia, after removing the metal layer outside the interconnect groove by chemical mechanical polishing so as to leave a metal interconnect in the interconnect groove, an organic acid cleaning treatment is carried out to the upper surface of the first insulation film and an upper surface of the metal interconnect, and wherein, thereafter, a hydrogen anneal treatment is carried out and thereafter a plasma treatment in an atmosphere including an ammonia gas is carried out, with an insulation copper diffusion barrier film being deposited by plasma chemical vapor deposition after the organic acid cleaning treatment, the hydrogen anneal treatment and the plasma treatment. See claim 2.

Furthermore, it is respectfully submitted that the teachings of the applied references would have neither disclosed nor would have suggested such fabrication method as in the present claims, having features as discussed previously in

connection with claim 2, and, additionally (but not limited to), wherein a reducing process is carried out after removing the metal layer by chemical mechanical processing but prior to carrying out the organic acid cleaning treatment (see claim 7), particularly wherein the reducing process is that set forth in claims 8-10; and/or wherein the metal layer is deposited by a plating technique (see claim 14); and/or wherein the first insulation film is an insulation film having a low dielectric constant not larger than 3 (see claim 15); and/or the further definition of formation of the insulation copper diffusion barrier film as in claims 16 and 17; and/or wherein citric acid (see claim 18), or a mixture of organic acid and hydrogen fluoride (see claim 19), is applied during the organic acid cleaning treatment; and/or wherein in the organic acid cleaning treatment any damaged layer in the upper surface is removed (see claim 20).

The present invention is directed to a method of fabricating a semiconductor integrated circuit device, particularly effective in connection with fabrication of a semiconductor integrated circuit device having buried interconnects with copper in the main conductor layers thereof. Recently, single and dual damascene techniques, for example, have been utilized for forming conductor layers, such that, respectively, the conductor layer is left only at an inside of an interconnect trench, and is left in a hole (for interconnection) and in the interconnect trench. Such techniques utilize chemical mechanical polishing so as to leave the conductor layer only at the inside of the trench (or in a hole and in the trench).

Recently, copper has been utilized as the conductor material in such techniques, having the advantage of lower resistance and greater allowable current in reliability. However, copper tends to more readily diffuse into an insulation film as compared to other metals; and, for this reason, it is necessary to form copper-

diffusion-preventing barrier films on the surface of the copper (e.g., on bottom and side surfaces), and it is also becomes necessary to form a cap film, for example, of silicon nitride, over the entire upper surface of an insulation film formed with an interconnection trench in such a manner as to cover the upper surface of the buried interconnect (except for electrical connection thereto), to prevent diffusion of copper from the upper surface of the buried interconnect.

Applicants have found various problems exist, when using copper as an interconnect material, with proposed techniques in forming interconnects as discussed previously. Specifically, Applicants have found that when using copper as an interconnect material, the time dependence on dielectric breakdown (TDDB) life is conspicuously short as compared to other metal materials (e.g., aluminum). Moreover, when using a low-dielectric-constant dielectric material which has recently been utilized in semiconductor devices, which is generally low in dielectric strength, there is still more difficulty in securing a sufficient TDDB life. Such conspicuously short TDDB life is a particularly difficult problem where the metal (e.g., copper) is deposited by a plating technique.

As to what is meant by TDDB, note, for example, Item 1 on pages 20-22 of Applicants' specification.

Upon further studies, by the present inventors, in using copper in a main conductor layer in a buried interconnect, Applicants have found additional problems arising, as described on pages 5 and 6 of Applicants' specification, causing a disadvantageous increase in interconnect resistance and/or disadvantageous separation between the interconnect layer of the buried interconnect and an insulation film (e.g., a cap film) formed thereover.

Against this background, and noting the problems found by the present

inventors, Applicants provide a process overcoming these problems. Specifically, Applicants have found that through use of a cleaning technique, after chemical mechanical polishing, wherein an organic acid cleaning treatment is carried out, thereafter a hydrogen anneal treatment is carried out, and thereafter a plasma treatment in an atmosphere including an ammonia gas is carried out, with an insulation copper diffusion barrier film being thereafter deposited by plasma chemical vapor deposition, problems found be Applicants and discussed on pages 4-6 of Applicants' specification can be avoided. In particular, TDDB life of the semiconductor integrated circuit device can be greatly improved.

To emphasize, the present invention defines a sequence of steps subsequent to chemical mechanical polishing, which greatly improves TDDB life and avoids disadvantageous increase in resistance. Note, for example, pages 66-75 of Applicants' specification; note also pages 109 and 110 thereof.

Mikagi discloses, inter alia, a method of making a semiconductor device with a trench interconnect that is buried into an interconnect trench formed in an organic insulation film, the process being described most generally at column 4, lines 1-33. This process includes forming inorganic insulation films on an organic insulation film in which is formed an interconnect trench; introducing nitrogen into surface parts of the inorganic insulation film; and burying a conductive material. The disclosed process in Mikagi avoids use of a barrier metal film. See column 8, lines 24-30. This patent discloses use of chemical mechanical polishing, in column 8, lines 40-47.

It is respectfully submitted that Mikagi does not disclose, nor would have suggested, the after treatments to the chemical mechanical polishing, of carrying out organic acid cleaning treatment, hydrogen anneal treatment and plasma treatment in

a gas atmosphere including an ammonia gas, in the sequence as in the present claims, and advantages thereof.

The Examiner contends on pages 2 and 3 of the Office Action mailed August 3, 2005, that Mikagi discloses various plasma treatments and deposition of a SiON layer/insulation copper diffusion barrier film. Note, however, that the plasma treatments referred to by the Examiner in Mikagi, are plasma treatments for introducing nitrogen into the protective films. It is respectfully submitted that such introduction of nitrogen is prior to chemical mechanical polishing of, e.g., copper formed through the respective protection film. It is respectfully submitted that Mikagi would have taught away from the presently claimed subject matter, including the steps and the sequence of these steps after removing the metal layer outside the interconnect groove by chemical mechanical polishing, and advantages thereof.

It is respectfully submitted that the additional teachings of Skee, et al. would not have rectified the deficiencies of Mikagi, such that the presently claimed invention as a whole would have been obvious to one of ordinary skill in the art.

Skee, et al. discloses a hydrogen peroxide-free cleaner for use in the microelectronics industry, for cleaning integrated circuit substrates of metal contamination while maintaining wafer surface smoothness. See column 1, lines 6-10. As a disclosed background thereto, this patent describes cleaning integrated circuit substrates utilizing initially an alkaline solution comprising a hot aqueous mixture of ammonium hydroxide, hydrogen peroxide and water; and subsequent thereto a hot acid solution treatment to remove metals untouched by the first treatment, the hot acid solution comprising hydrogen peroxide, hydrochloric acid and water. This patent goes on to disclose problems arising in connection with utilizing hydrogen peroxide-containing compositions, and discloses a process for cleaning

wafer substrate surfaces utilizing a hydrogen-peroxide-free, aqueous cleaning solution including an alkaline, metal ion-free base and a polyhydroxy compound containing from 2-10-OH groups. See column 4, lines 10-32. Note also column 5, lines 5-32, describing various alkaline components that may be used in the cleaner compositions; and column 6, lines 1-23 and 44-47 describing additional components that may be included in the cleaning compositions.

It is emphasized that Skee, et al. discloses a cleaning solution of an alkaline, metal ion-free base and a polyhydroxy compound. It is respectfully submitted that the teachings of this reference, even in combination with the teachings of Mikagi, would have neither taught nor would have suggested, and in fact would have taught away from, such a post chemical mechanical polishing treatment as in the present claims, including, inter alia, the organic acid cleaning treatment, much less such organic acid cleaning treatment together with the hydrogen anneal treatment and plasma treatment in an atmosphere including an ammonia gas, in the sequence as in the present claims, and advantages thereof.

The contention by the Examiner on page 3 of the Office Action mailed August 3, 2005, that Skee, et al. discloses a method for cleaning wafers that includes the step of using an alkali solution containing aminoethanol and a cleaning treatment using an acid solution, is noted. However, it is respectfully submitted that the additional components referred to in column 6, lines 1-23, of Skee, et al., are additional components used as metal chelating agents included in the alkaline cleaner compositions, not a separate cleaning composition. It is respectfully submitted that Skee, et al. would have neither taught nor would have suggested such organic acid cleaning treatment as in the present claims, much less such organic acid cleaning treatment together with the other recited steps as discussed

previously, in the recited sequence.

Ngo, et al. discloses a method of manufacturing a semiconductor device including copper or copper alloy metallization, wherein a dielectric layer is formed overlying a substrate; an opening is formed in the dielectric layer; a layer of copper or copper alloy is deposited over the dielectric layer; chemical mechanical polishing is performed, leaving the exposed surface of the copper or copper alloy layer oxidized; the exposed surface of the copper or copper alloy layer is treated with a hydrogen-containing plasma to substantially reduce the exposed oxidized surface; the surface treated with the hydrogen-containing plasma is reacted with silane or dichlorosilane to form a layer of copper silicide on the treated surface; and a capping layer of silicon nitride is deposited on the copper silicide layer. Note column 4, lines 18-32. See also column 4, lines 12-17. Note further column 5, lines 27-34; and column 6, lines 59-63.

Even assuming, arguendo, that the teachings of Ngo, et al. were properly combinable with the teachings of Mikagi and Skee, et al., it is respectfully submitted that such combined teachings would have neither disclosed nor would have suggested the presently claimed subject matter, including, inter alia, after the chemical mechanical polishing, carrying out organic acid cleaning treatment, much less carrying out the organic acid cleaning treatment together with the hydrogen anneal treatment and plasma treatment in the atmosphere including an ammonia gas, especially in the sequence of these steps as recited in the present claims, and advantages thereof.

In view of the foregoing comments and amendments, reconsideration and allowance of all claims presently pending in the above-identified application are respectfully requested.

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Respectfully submitted,

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